REMARKS

Claims 1-11 remain pending in this application with claims 1 and 3 being amended and claims 2, 8, 9 and 11 being cancelled by this response. The features of cancelled claim 2 has been added to amended claim 1. Claim 3 has been amended to be dependent on claim 1. Applicant respectfully submits that no new matter is added by amended claims 1 and 3.

Rejection of claims 1-11 under 35 U.S.C. 102(e)

Claims 1-11 are rejected under 35 U.S.C. 102(e) as being anticipated by Valmiki et al. (U.S. Patent No. 6,636,222 hereinafter Valmiki).

The present invention as claimed in claim 1 provides an electronic apparatus. A graphics memory stores a first and second graphics object. An OSD processor generates a first digital stream representing the first graphics object and a pictures memory contains a picture and generates a second digital stream. A mixer is able to mix the first digital stream and the second digital stream into a video signal. The second graphics object is converted into picture data by a device for converting. The picture data is written to the picture memory by a device for writing. Overlaps between the first and second graphics objects are detected by a device for detecting generating an overlap cue.

A process for generating a video signal is provided in claim 10. In this process, a command to display a first and second graphics object is received. Detection of a possible overlap between the first and second graphics object takes place. In the absence of an overlap, a digital stream representing the first graphics object and the second graphics is generated by an OSD processor, and the generation of a video signal based on the digital stream takes place. If there is the presence of an overlap, a first digital stream representing a first graphics object generated by an OSD process takes place. The second graphics object is converted into a picture. The picture is written to a memory. The generation of a second digital stream from the memory takes place. The mixing of the first digital stream and of the second digital stream takes place. The generation of a video signal from said mixture takes place.

Some OSD processors are limited in their capacity to manage the OSD plane. In particular, they do not make it possible for the display of two graphics objects which share the same lines of the screen. The present invention relates to a method for enabling the display of two graphics sharing the same lines of a screen while using an OSD processor.

Valmiki describes a video and graphics system which processes video data including both analog video, e.g., NTSC/PAL/SECAM/S-video, and digital video, e.g., MPEG-2 video in SDTV or HDTV format. The video and graphics system includes a video decoder, which is capable of concurrently decoding multiple SLICEs of MPEG-2 video data. The video decoder includes multiple row decoding engines for decoding the MPEG-2 video data. Each row decoding engine concurrently decodes two or more rows of the MPEG-2 video data. The row decoding engines have a pipelined architecture for concurrently decoding multiple rows of MPEG-2 video data. The video decoder may be integrated on an integrated circuit chip with other video and graphics system components such as transport processors for receiving one or more compressed data streams and for extracting video data, and a video compositor for blending processed video data with graphics.

Valmiki deals generally with a system enabling the display of two graphics sharing the same lines of a screen. The Office Action asserts that Valmiki describes an electronic apparatus with "means for detecting overlaps between the first and second graphics objects generating an overlap cue" in Column 13, lines 3-21. Applicant respectfully disagrees. Valmiki neither discloses nor suggests a system with an OSD processor. Valmiki describes a system where graphics windows may be displayed so they may overlap or cover each other with arbitrary spatial relationships. The windows overlap with a parallel graphics processing architecture. (Fig. 69) In particular, 4 pipelines are used, and they are not managed by a single processor. Although the passage cited in the office Action describes that graphics windows may be displayed such that they may overlap or cover each other, this passage nor elsewhere in Valmiki is it disclosed or suggested that overlaps between the first and second graphics objects are detected generating an overlap cue. Valmiki is not at all concerned with detection of the overlaps nor the objectives of the present claimed invention, enabling the display of two graphics sharing the same lines of a screen while using an OSD processor. Thus, Valmiki neither teaches nor suggests "means for detecting overlaps between the first

and the second graphics objects generating an overlap cue" as recited in amended claim 1 of the present invention.

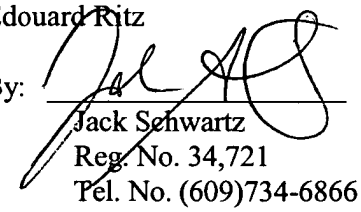
Valmiki neither discloses nor suggests an OSD processor that performs the detection of the window overlap. Since the detection of the window overlap is neither disclosed nor suggested, Valmiki cannot disclose or suggest "detection of a possible overlap between the first and the second graphics object" as recited in claim 10 of the present claimed invention. It thus follows that Valmiki cannot disclose or suggest the method steps for the detection of the window overlap. Thus, Valmiki neither discloses nor suggests "if presence of an overlap: generation by an OSD processor of a first digital stream representing a first graphics object; conversion of the second graphics object into a picture; writing of the picture to a memory; generation of a second digital stream from the memory; mixing of the first digital stream and of the second digital stream" as recited in claim 10 of the present claimed invention.

In view of the above remarks and amendments to claim 1, it is respectfully submitted that Valmiki provides no 35 USC 112 enabling disclosure that anticipates the invention claimed in claims 1 and 10. As claims 3 – 7 are dependent on claim 1, Applicant respectfully submits that claims 3- 7 are also not anticipated by Valmiki. Therefore, if is further respectfully submitted that this rejection has been satisfied and should be withdrawn.

Having fully addressed the Examiner's rejections, it is believed that, in view of the amendments and remarks, this application stands in condition for allowance. Accordingly then, reconsideration and allowance are respectfully solicited. If, however, the Examiner is of the opinion that such action cannot be taken, the Examiner is invited to contact the applicant's attorney at the phone number below, so that a mutually convenient date and time for a telephonic interview may be scheduled.

No additional fee is believed due. However, if a fee is due, please charge the fee to Deposit Account 07-0832.

Respectfully submitted,
Edouard Ritz

By: 

Jack Schwartz
Reg. No. 34,721
Tel. No. (609)734-6866

Thomson Licensing, LLC
Patent Operations
PO Box 5312
Princeton, NJ 08543-5312
January 23, 2008

CERTIFICATE OF MAILING under 37 C.F.R. §1.8

I hereby certify that this amendment is being deposited with the United States Postal Service as First Class Mail, postage prepaid, in an envelope addressed to Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on:

Date: January 23, 2008

Jack Schwartz
Reg. No. 34,721